# Network with Programmable Interconnect Node

## ABSTRACT

A circuit having an interconnect network and plurality of processing blocks is disclosed. The interconnect network has a plurality of network nodes arranged in a two-dimensional array on a first substrate. Each network node has a plurality of communication ports and is connected to each adjacent network node by a communication bus that connects only those two network nodes and processing blocks adjacent to that communication bus. A programmable switch within each node connects one of the input ports to one of the output ports in response to connection information stored in a memory in that node. Three-dimensional embodiments can be constructed by including a second substrate that overlies the first substrate and includes a second such interconnect network that is connected vertically through one or more nodes. The circuit easily accommodates spare processing blocks that can be substituted for defective blocks by altering the connection information.